

Docket No.: **4698-039**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : ATTN: Certificate of Correction Branch
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Inventors: Biing-Seng WU et al. :
:
U.S. Patent Application No. 7,221,350 : Group Art Unit: 2673
: Allowed: November 16, 2006
Issue Date: May 22, 2007 : Examiner: NITIN PATEL
:
:

For: METHOD OF REDUCING FLICKERING AND INHOMOGENEOUS BRIGHTNESS
IN LCD

**REQUEST FOR CERTIFICATE OF CORRECTION OF
OFFICE MISTAKE UNDER 37 CFR 1.322**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reviewing the above-identified patent, errors on the part of the Patent and Trademark Office was discovered. Correction is required in order to conform with the Patent to the Official Record in the application.


The errors noted is set forth on one attached copy of form PTO-1050 Rev. 2-93 in the manner required by the Commissioner's Notice.

The change requested herein corrects an error of the Patent and Trademark Office and the Certificate should be issued without expense to the patentee under Rule 1.322 of the Rules of Practice. Accordingly, issuance of the Certificate of Correction is requested.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**Page 1 of 1

PATENT NO. : 7,221,350

APPLICATION NO.: 09/826,096

ISSUE DATE : May 22, 2007

INVENTOR(S) : WU et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Cover page, Item (73) Assignee:

Please amend Assignee's name as follows from "Chi Mai Optoelectronics" to --CHI MEI OPTOELECTRONICS CORP.--

Column 6, Line 9 of Claim 6:

Please amend the Line 9 as follows from:

"gate voltage deformation means for, generating a" to --gate voltage deformation means for generating a--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

LOWE HAUPTMAN HAM & BERNER LLP
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Alexandria, VA 22314

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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US007221350B2

(12) **United States Patent**
Wu et al.

(10) **Patent No.:** **US 7,221,350 B2**
(45) **Date of Patent:** **May 22, 2007**

(54) **METHOD OF REDUCING FLICKERING AND INHOMOGENEOUS BRIGHTNESS IN LCD**

(75) Inventors: **Biing-Seng Wu**, Hsin-Shih Village (TW); **Wen-Jyh Sah**, Hsin-Shih Village (TW); **Chao-Wen Wu**, Hsin-Shih Village (TW)

→ (73) Assignee: **Chi-Mei Optoelectronics Corp.** (TW) ←

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1074 days.

(21) Appl. No.: **09/826,096**

(22) Filed: **Apr. 5, 2001**

(65) **Prior Publication Data**

US 2001/0028337 A1 Oct. 11, 2001

(30) **Foreign Application Priority Data**

Apr. 6, 2000 (TW) 89106352 A

(51) **Int. Cl.**
G09G 3/36 (2006.01)

(52) **U.S. Cl.** 345/92; 345/93

(58) **Field of Classification Search** 345/82, 345/83, 87, 88, 89, 90, 91, 92, 93, 94, 95-100, 345/204; 327/91, 141

See application file for complete search history.

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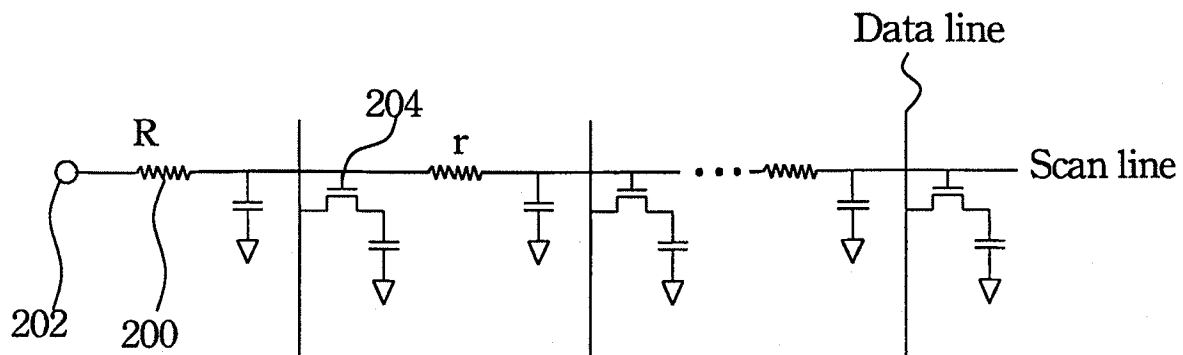
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Primary Examiner—Nitin Patel

(57) **ABSTRACT**

A method of reducing flickering and inhomogeneous brightness in an LCD. The method serially connects each scan line connecting a plurality of pixels in a row with a resistor to form a scan line circuit. The resistor is connected between the first pixel of the scan line and the voltage input terminal of the scan line, so that the gate voltage entering the TFT in the first pixel deforms. The voltage of the TFT decreases when it is turned off, minimizing screen flickering and inhomogeneous brightness due to the capacitor charge coupling effect between the first pixel and the last pixel on a scan line.

10 Claims, 5 Drawing Sheets



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What is claimed is:

1. A scan line circuit that solves screen flicker, imperfect exposure junctions and inhomogeneous brightness in a TFT-LCD, which includes a plurality of perpendicular scan lines and a plurality of horizontal data lines, each of the scan lines connecting a plurality of pixel TFTs in a row and each of the data lines connecting a plurality of pixel TFTs in a column to form an array of the pixel TFTs, and a drain of the each pixel TFTs connecting a liquid crystal capacitor and a storage capacitor, wherein each of the scan line comprises:
 - gate voltage deformation means for deforming a gate input voltage waveform input from an input terminal of the scan line, the gate voltage deformation means located only between the gate of the first pixel TFT in the row and the input terminal of the scan line.
2. The circuit of claim 1, wherein the gate voltage deformation means comprises a resistor.
3. The circuit of claim 2, wherein the resistance of the resistor is in the range between 10 Ω /sq and 100 Ω /sq.
4. The circuit of claim 1, wherein the gate voltage deformation means comprises an ITO thin film.
5. The circuit of claim 1, wherein the gate voltage deformation means comprises a TFT that the TFT's gate connects the TFT's source directly.
6. A scan line circuit that solves screen flicker, imperfect exposure junctions and inhomogeneous brightness in a TFT-

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LCD, which includes a plurality of perpendicular scan lines and a plurality of horizontal data lines, each of the scan lines connecting a plurality of pixel TFTs in a row and each of the data lines connecting a plurality of pixel TFTs in a column to form an array of the pixel TFTs, and a drain of the each pixel TFTs connecting a liquid crystal capacitor and a storage capacitor, wherein each of the scan line comprises:

gate voltage deformation means for generating a deformed gate voltage waveform transmitted to the pixel TFTs connected to the same scan line, the gate voltage deformation means located between the gate of the first pixel TFT in the row and the input terminal of the scan line.

7. The circuit of claim 6, wherein the gate voltage deformation means comprises a resistor.
8. The circuit of claim 7, wherein the resistance of the resistor is in the range between 10 Ω /sq and 100 Ω /sq.
9. The circuit of claim 6, wherein the gate voltage deformation means comprises an ITO thin film.
10. The circuit of claim 6, wherein the gate voltage deformation means comprises a TFT that the TFT's gate connects the TFT's source directly.

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